Amendments to the Drawings:

The drawing sheets attached in connection with the above-identified application containing Figures 1-21 are being presented as new formal drawing sheets to be substituted for the previously submitted drawing sheets. All drawing figures have been amended to more clearly illustrate various aspects. The figures have been amended to include text greater than 1/8 inch in height. In addition, Figure 4 has been corrected to recite "Iteration N" in state 40, and "Iteration N+2" in state 44. In Figure 14, both occurrences of "Intermdiate" have been amended to "Intermediate." In Figure 18, the word "received" has been corrected.

REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 4, 6-8, 11-15, 25, 29 and 31 are currently being amended.

Claims 32-33 are currently new.

Claim 22 was previously canceled.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1-21 and 23-333 are now pending in this application.

Objections to the Drawings

The drawings were objected to under 37 C.F.R. 1.84 (p) for having text or numbers less than 1/8 inch in height. Applicant has amended Figures 1-21 to address this objection.

Further, the Examiner objected to the drawings for not mentioning reference characters 16 and 18 in Figure 1 as well as reference character 60 in Figure 7. Applicant respectfully notes that reference character 16 may be found in paragraph [0006] of the specification, and that reference character 60 may be found in paragraph [0054] of the specification. Reference character 18 has been removed.

The Examiner also objected to the drawings as allegedly not showing every feature specified in the claims. Specifically, the Examiner alleges that the power controller recited in claims 8 and 25 is now shown. Applicant has amended claims 8 and 25 to clarify this feature, an embodiment of which is described within Paragraph [0042] and illustrated in Figure 2 (e.g., processor 20).

The Examiner further alleges that the figures lack an output memory buffer recited in claims 11 and 29. Applicant respectfully notes that, as understood by those skilled in the art, an output memory buffer may be any buffer receiving an outputted result. As such, a secondary memory buffer, intermediate results buffer, or any similar type buffer may be considered an output memory buffer. The figures clearly illustrate such buffers at, for example, Figure 7 (reference numeral 54) and Figure 10 (reference numeral 86).

Further, the Examiner alleges that the circuitry to perform searches as recited in claim 12 is lacking in the figures. However, as disclosed in the originally filed specification, the processor may utilize numerous types of fingers, or algorithms, in order to perform searches. Thus, as illustrated in Figure 16, for example, the searcher located in the processor may perform such a function.

Finally, the Examiner alleges that the plurality of distinct receiver chains, as recited in claim 17, is lacking in the Figures. However, as noted in the specification at paragraph [0072], the buffer (x2) 22 illustrated in Figure 13 is representative of an element which may handle more than one RF chain.

Accordingly, the objections to the drawings should be withdrawn.

Claim Objections

Claims 6 and 15 were objected to for certain informalities. Applicant has amended these claims in order to more clearly recite the invention. Thus, Applicant requests these objections be withdrawn.

Rejections under 35 U.S.C. 112, first paragraph

Claims 3, 4, 6, 13-15, 20-21 and 23-29 were rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. Applicant respectfully traverses the rejection for at least the following reasons.

Regarding claim 3, the Examiner alleges that because the word "defining" is not found in the detailed description with regards to the demodulation process, "it is still unclear how the iteratively accumulating step 'defines' a demodulation operation." Office Action

dated June 6, 2008, Page 10. Applicant respectfully notes that the accumulating step may define the demodulation operation because, as recited in claim 1, accumulating the correlated component into the second memory element provides a particular correlated multi-path element from the signal (e.g., demodulation). Demodulation is defined by taking an original modulated signal (e.g., signal with specific characteristics associated with it), and changing the signal into a signal in which the system may process it. Accordingly, the specific parameters in which the demodulator functions are what define the demodulation process. Thus, as recited in claim 1, "a method for demodulation of a composite signal," the steps of buffering digital samples and randomly accessing the digital samples also affect the demodulation process. However, correlating the particular multipath component from the signal (i.e., manipulating a part of the modulated signal) and then, finally accumulating this correlated (e.g., specific parameter) signal at the second memory element defines that the signal at the second memory element is a demodulated signal and that the operation, provided through the method of claim 1, is completed. Therefore, the iteratively accumulating of the particular component defines the demodulation operation recited in claim 3.

Further, the Examiner alleges that "using information from the signal to determine the amount of demodulation processing" is "unclear as the what information is used from the signal and how the amount of processing changes based on this information." Office Action dated June 6, 2008, Page 10. Applicant respectfully notes that the original modulated signal would determine the amount of processing necessary. Dependent on the size, frequency, or similar component of the received signal (i.e., information from the signal), it be clear to one skilled in the art as describing the amount of components that would be correlated from it. Accordingly, depending on this information, the demodulation process would be known, because the entire signal, not portions thereof, would be demodulated within the demodulation operation clearly claimed within claim 1. For example, if the entire composite signal "containing a plurality of multipath components" had been demodulated, there would be no "digital samples of a signal" left from which to correlate a particular multipath component. Thus, the demodulation process would end and the amount of processing would be determined. Since the above-noted operation would be understood by those skilled in the art in light of the description provided in the specification, claim 3 is sufficiently enabled.

Regarding claim 4, the Examiner alleges that the cited portions of the present specification only provide dynamic processing ability of a single processing unit. However, as previously noted by Applicant, paragraphs [0042]-[0046] of the originally filed specification describe an exemplary embodiment of the present invention. Paragraph [0042] discloses:

> "[T]he processor 20 is configured to provide dynamic path processing. This dynamic path processing may be referred to as a "virtual finger" feature because the multi-path communications paths, or fingers, are … paths defined using various algorithms."

Accordingly, claim 4 recites that this determination of the component may "vary dynamically between processing units" because the various algorithms utilized for this dynamic processing in a processor. Again, the aforementioned paragraph recites an embodiment for one exemplary processing unit, thus the accumulation may vary dynamically throughout different processing units.

The Examiner repeats the earlier rejection of claims 6 and 15. In a previous reply Applicant mistakenly directed the Examiner's attention to paragraphs [0058]-[0065]. Applicant respectfully notes that attention should be directed to Figure 17 and paragraphs [0082] and [0084]-[0087] of the present application. The features recited in claims 6 and 15 are clearly described in these portions of the originally filed specification and figures.

Claim 13 was rejected by the Examiner because the disclosure allegedly does not describe how additional limitations in the claim interface with the elements of the parent claim 7. In addition to various other limitations already present in claim 13, Applicant has amended claim 13 to recite that the "plurality of buffers comprises separate sets of physical buffers for even and odd digital samples …."

Regarding, claim 14, the Examiner alleges that the permutation block itself is not being selected. In accordance with the Examiner's suggestions, Applicant has amended claim 14 to clarify this selection.

The Examiner rejected claim 20 under 35 U.S.C. 112, first paragraph, as allegedly being unclear how to provide a despreader "adaptable to arbitrary sample rates and symbol

time." Applicant directs the Examiner's attention to paragraph [0064] of the present application and respectfully notes that it would be clear to one skilled in the art that, in a conventional despreader, which is not run on a clock, the inconsistency of the input would not affect the functionality of the despreader itself. Thus, as the Examiner states "the claims language (i.e., 'adaptable') suggests the despreader is modified or adapted for different (i.e. inconsistent, arbitrary) sample rates and symbol times."

The Examiner rejected claim 21 as allegedly providing a limitation not found in the description of the present invention. Specifically, the Examiner objects to the recitation of "dynamically selecting" in claim 21. However, the dynamic selection of the algorithm, as recited in claim 21, is clearly described in the originally filed specification at, for example, paragraphs [0042]-[0046] and [0058], as well as in Figure 8. Further, paragraph [0064]-[0065] describe exemplary formulas for such calculations. Thus, the dynamically selecting an algorithm for accumulation via the channel estimate is sufficiently disclosed in the originally filed specification.

Accordingly, Applicant respectfully requests that these rejections under 35 U.S.C. § 112, first paragraph, be withdrawn.

Rejections under 35 U.S.C. § 112, second paragraph

Claims 4, 6-7 13-15, 20, 21 and 23-29 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. Applicant respectfully traverses the rejection for at least the following reasons.

The Examiner rejected claim 4 as being unclear as to how the determination step and the processing units relate to the steps of claim 1. Further, the Examiner rejected claim 4 as being unclear whether the multi-path components recited are related to the multi-path component of claim 1. Applicant refers to the arguments presented in Applicant's previous response. Further, Applicant has amended claim 4 to more clearly recite these features.

Next, the Examiner rejected claims 6 and 15 as allegedly being unclear as to "operating on the digital samples of the original frequency." As noted above, Applicant

believes that, in view of the detailed description at paragraphs [0084]-[0087], the claimed feature would be clearly understood by one skilled in the art.

The Examiner rejected claim 7 for alleged inconsistencies between the claim language, the detailed description and Figures 7 and 13. Applicant has amended claim 7 in accordance with the Examiner's suggestion.

Regarding claim 12, the Examiner alleges that Applicant explains the timing hypothesis but fails to address the claimed language to indicate which signal is being correlated with it. As previously stated, claim 12 recites that the circuitry within the apparatus attempts to locate and correlate these multi-path components based on a hypothesis, such as an algorithm which is formulated with various factors, of where they will be at specific times, hence "timing hypothesis." Applicant has amended claim 12 to more clearly recite this feature.

The Examiner rejected claim 13 for reasons similar to those stated above. Applicant refers to the arguments above addressing those rejections.

Next, the Examiner rejected claim 30 under 35 U.S.C. § 112, second paragraph, as allegedly being unclear as to how "demodulating" relates to the asynchronous processing. Applicant respectfully notes that it would be clear to one skilled in the art that the demodulating of the waveform is accomplished through processing of the sample. Accordingly, the specific difference in demodulating this particular waveform is due to 1) the asynchronous processing and 2) the processing based on programmed instructions, as recited in claim 30.

Claim 31 was rejected by the Examiner as allegedly being vague and indefinite for incorrectly reciting "demodulating process." Applicant has amended claim 31 to more clearly recite the claimed features.

Accordingly, Applicant respectfully requests that these rejections under 35 U.S.C. § 112, second paragraph, be withdrawn.

Rejections under 35 U.S.C. 102

Claims 1, 2, 30 and 31 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 6,985,516 to Easton ("Easton"). Applicant respectfully traverses this rejection for at least the following reasons.

Embodiments of the present invention relate to an improved method of demodulating multi-path signals with a virtual finger method and an apparatus for processing digital communication signals through common circuitry for both transmit and receive operations in a digital communication system. Independent claim 1 recites a "method for demodulation of a composite signal containing a plurality of multi-path components" that comprises "buffering digital samples of a signal into a first memory element" and "randomly accessing the digital samples from the first memory element to correlate a multi-path component from the signal."

Easton as noted by the Examiner, relates to a system of how samples are retrieved and processed. For instance, Easton discloses "a particular segment of samples can be retrieved from the buffer and processed." Easton, col. 14, lines 4-5. Easton further discloses that the segments are limitedly chosen based on the coherency during a period of time. In addition, Easton discloses another option for accessing the samples, where they are sequentially retrieved based on time offset of the segments stored within the buffer. Easton, col. 14, lines 26-40. The Examiner argues that Easton's disclosure does not suggest sequential retrieving of the samples, but rather processing. See Office Action dated June 6, 2008, page 7. Applicant respectfully disagrees with the Examiner's interpretation of the disclosure of Easton.

Applicant respectfully notes that Easton discloses:

> "Segments of data samples ... can be sequentially processed. For example, samples … may be retrieved from buffer 224 and processed by data processor 230. Upon completion of the processing …, another segment of samples (e.g., corresponding to the second multipath) can be retrieved from buffer 224 and processed." Easton, col. 14, lines 26-33 (emphasis added).

Accordingly, Easton discloses this sequential processing is necessary for retrieval and subsequent processing based on time offset of the segments stored within the buffer.

Therefore, the starting samples being processed cannot correspond to any location in the buffer, as alleged by the Examiner. Thus, Easton fails to teach or suggest at least this feature and, in fact, teaches away from samples being randomly accessed.

Claims 1 and 2 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 7,035,318 to Taniguchi *et al.* ("Taniguchi"). Applicant respectfully traverses this rejection for at least the following reasons.

As is the case with Easton, Taniguchi also fails to teach or suggest at least the above-noted feature. The Examiner alleges that "since the buffer is read non-sequentially, the circuit in Taniguchi is randomly accessing the digital samples." Office Action dated June 6, 2008, page 15. The Examiner further cites to column 8, lines 33-44 and column 10, lines 39-62 as disclosing this feature. However, Taniguchi describes the usage of a generated read pointer, which is supplied to the input buffer. See Taniguchi, col. 8. Further, in accordance with the disclosure of Taniguchi, the read pointer, which is time dependent (i.e., sequential) determines the order in which each signal is read from the RAMs to be selected by a selector (52h) before being written to the despreading finger section. Taniguchi discloses that timing information associated with each multipath component is provided to an external register, where it is stored and added together with a count value output by means of a microscheduler. See Taniguchi, col. 8, lines 33-44. This is further described through FIG. 8 and column 9 of Taniguchi, which demonstrates that the selection of data occurs according to a specific set of criteria, not randomly as disclosed within the present invention. Accordingly, Taniguchi discloses a different method for selecting data from a buffer and fails to teach or suggest the above-noted feature of the pending claims.

Accordingly, independent claims 1 and 30 are patentable. Claims 2 and 31 each depend from one of allowable claims 1 or 30 and are, therefore, patentable for at least that reasons, as well as for additional patentable features when those claims are considered as a whole.

Rejections under 35 U.S.C. § 103

The Examiner rejected claim 5 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Taniguchi in view of U.S. Publication No. 20030235238 to Schlem *et al.* ("Schlem"). The Examiner has rejected claim 6 over Easton in view of Taniguchi and further in view of U.S. Patent No. 6,748,010 in the name of Butler *et al.* (hereinafter "Butler"). Claims 5 and 6 depend from allowable claim 1 and are, therefore, patentable for at least that reasons, as well as for additional patentable features when those claims are considered as a whole.

The Examiner rejected claims 7-10, 19-20 and 22-27 as being unpatentable over Taniguchi in view of Schlem. Applicant respectfully traverses this rejection for at least the following reasons.

As noted above by Applicant, the prior art teaches away from the features recited in the pending claims. Specifically, Taniguchi fails to teach or suggest random accessing of samples from a first memory element. Further, Taniguchi discloses an explicit manner in which the samples are written into a plurality of RAMs and then read from them. Thus, in addition to failing to teach or suggest this feature, Taniguchi teaches away from this feature. Furthermore, Schlem fails to cure this deficiency.

Instead, Schlem discloses "a receiving unit for receiving CDMA system signals" and "semiconductor device for processing CDMA system signals." Accordingly, Schlem primarily teaches how to handle such estimation of channel tap elays in a CDMA receiving procedure. This system both lacks the ability to handle both composite, spread spectrum, signals in a multipath environmnet and transmission thereof within common circuitry as taught within the present invention. Accordingly, Schlem teaches that the samples are written into and read from a rake receiver from a matched filter. This read/write process is based on a code sequence assigned to the receiver, with controlled timing of each finger. (See, Schelm, Paragraphs [0026], [0052], [0057], Figures, 2-5). Thus, Schelm fails to teach not only the specified improvement of common circuitry, but also the random access capabilities therein. Therefore, 7 and 20 are patentable.

In order to establish a prima facie case of obviousness, "... the prior art reference (or references when combined) must teach or suggest all the claim limitations." See M.P.E.P. § 2142, ¶1 (underlining added). Accordingly, Applicant respectfully requests these rejections to be withdrawn.

Next, the Examiner rejected claims 11 and 29 under 35 U.S.C. § 103 (a) as being unpatentable over Taniguchi in view Schlem and further in view of U.S. Publication No. 2001/0036195 in the name of Garyantes *et al.* (hereinafter "Garyantes"). The Examiner rejected claims 15-16 under 35 U.S.C. § 103 (a) as being unpatentable over Taniguchi in view Schlem and further in view of Butler. The Examiner rejected claims 17 and 28 under 35 U.S.C. § 103 (a) as being unpatentable over Taniguchi in view Schlem and further in view of Easton. The Examiner rejected claims 18 under 35 U.S.C. § 103 (a) as being unpatentable over Taniguchi in view Schlem and further in view of U.S. Publication No. 2003/0128678 in the name of Subrahmanya *et al.* (hereinafter "Subrahmanya"). Finally, The Examiner rejected claim 28 under 35 U.S.C. § 103 (a) as being unpatentable over Taniguchi in view Schlem and further in view of Subrahmanya and Easton.

Claims 8-11, 15-19, 23-26 and 28-29 each depend, either directly on indirectly, from one of allowable claims 7 or 20 and are, therefore, patentable for at least that reason, as well as for additional patentable features when those claims are considered as a whole.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by the credit card payment instructions in EFS-Web being incorrect or absent, resulting in a rejected or incorrect credit card transaction, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely

acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date 6 October 2008

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